**CHAPTER 6**

**SIMULATIONS AND RESULTS**

In this chapter all the properties of the 4T and 6T SRAM cell are compared. The specifications of the tool and technology used are mentioned as follows.

**Tool:** Microwind **Technology:** 50 nm (2λ)

VDD = 0.5V VTH = 0.2V

To make the comparison two memory blocks are designed, one with standard 6T cell and one with the proposed 4T cell. Each block contains 128 bytes and total of 16 bit-lines (and inverse bit-lines for the 6T case), where each bit-line is connected to 8 cells. These bit-lines are then multiplexed into a 8 bit word and given as input to the sense ampliﬁers.

In the memory block each column contains only 8 cells. The effect of divided bit line technique cannot be evaluated if it is implemented on such a small bit line. Usually cache memory blocks are of size 1KB. In order to implement and evaluate the divided bit line technique a single column of 128 cells is designed with all peripheral circuits. These cells are grouped into sets of 12 cells as discussed in chapter 5.

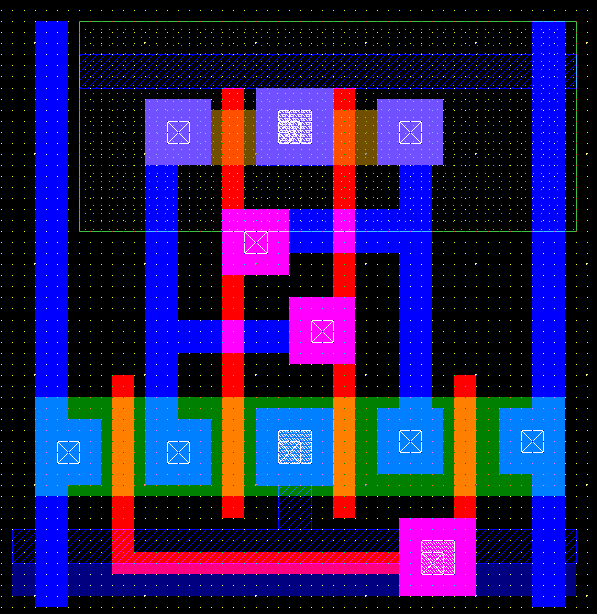
Simulation results for different modules for 4T and 6T SRAMs are as follows.

**6.1 SINGLE CELL COMPARISON**

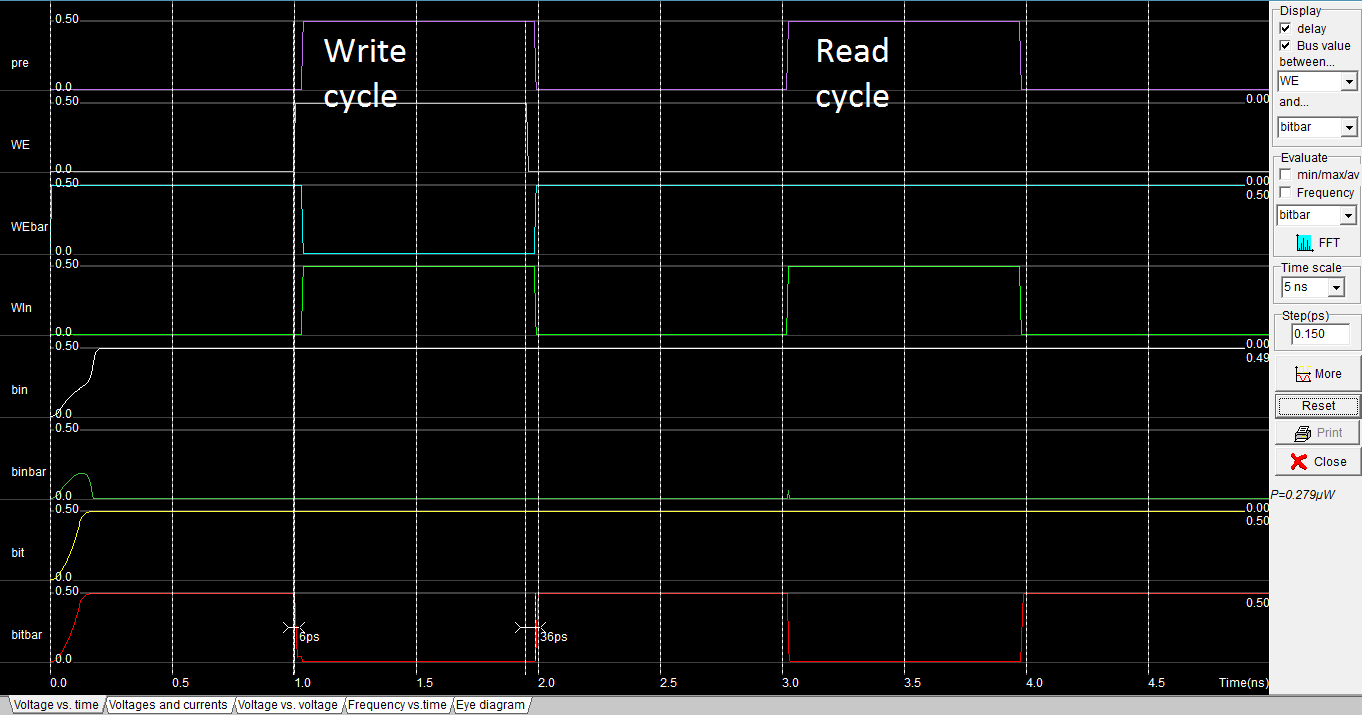
|  |  |  |
| --- | --- | --- |
| Parameter | 6T | 4T |
| Avg. Write power | 0.551µW | 0.349µW |
| Avg. Read power | 0.198µW | 0.171µW |
| Avg. Static power | 0.114µW | 0.0995µW |
| Cell delay(write 1) | 0.02nS | 0.034nS |
| Cell delay(write 0) | 0.013nS | 0.065nS |

**Table [6.1] Single cell simulation results for 6T and 4T SRAM**

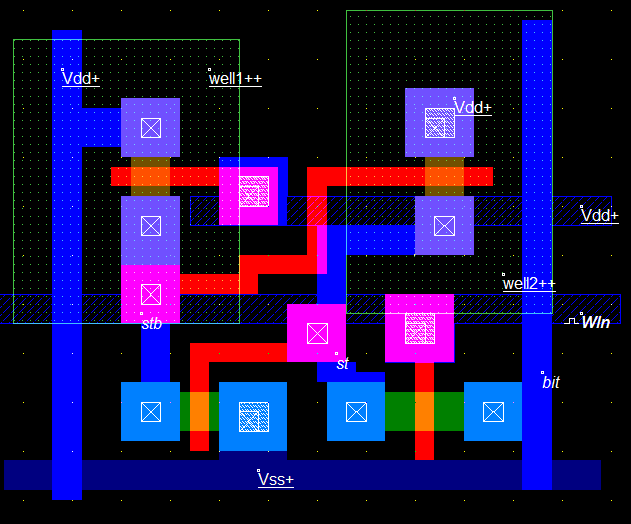
Write power and read power are reduced by 36% and 10.5% and static power is reduced by 13% in 4T SRAM. Cell delay of 4T SRAM for write '1' is 70% more and for write '0' is five times that of 6T SRAM. This is the main drawback of 4T SRAM making it inappropriate to replace 6T SRAM in practical applications.



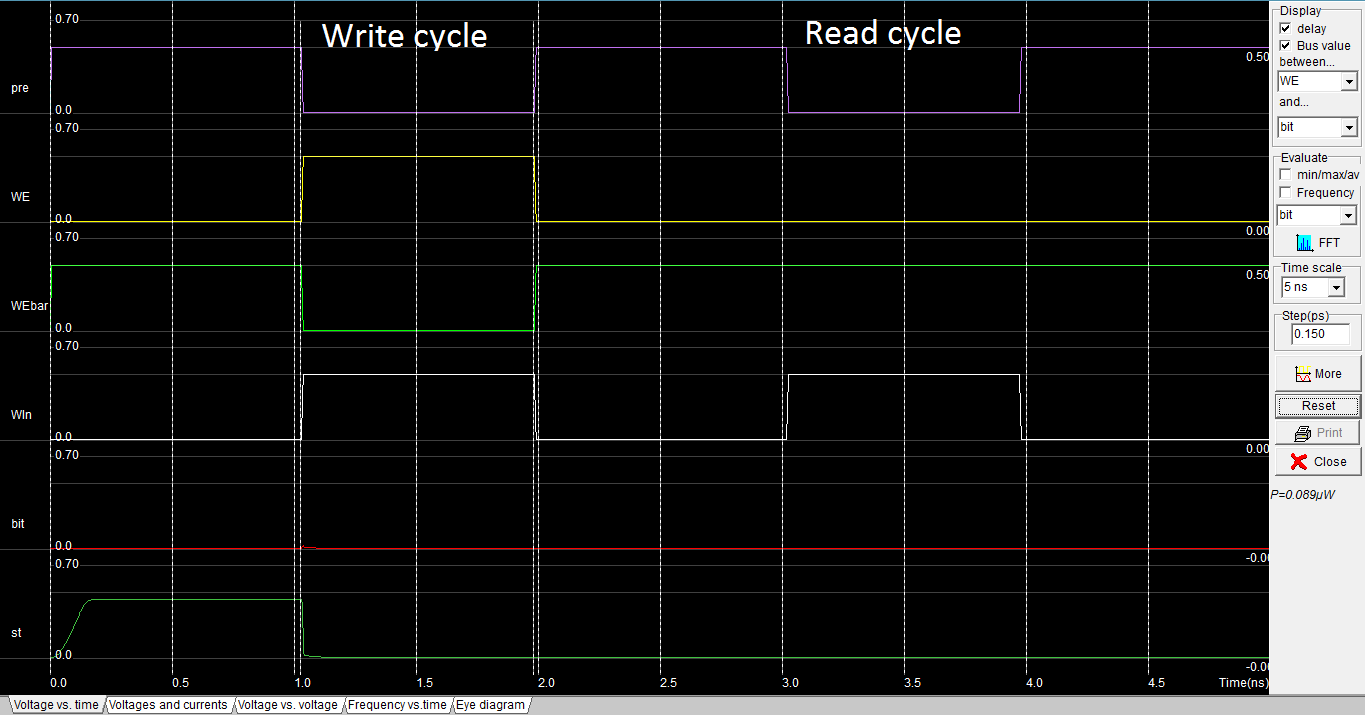
**Fig (6.1) Layout of 6T SRAM cell**



**Fig (6.2) Simulation waveforms for 6T SRAM cell**



**Fig (6.3) Layout of 4T SRAM cell**

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**Fig (6.4) Simulation waveforms for 4T SRAM cell**

**6.2 CACHE COMPARISON**

When SRAM cells are placed in an array, power and delay parameters get affected due to the addition peripheral circuitry. This factor is very important as it alters the power and delay parameters of SRAM cell. The following results evaluate the power and delay parameters of 6T and 4T SRAM cache.

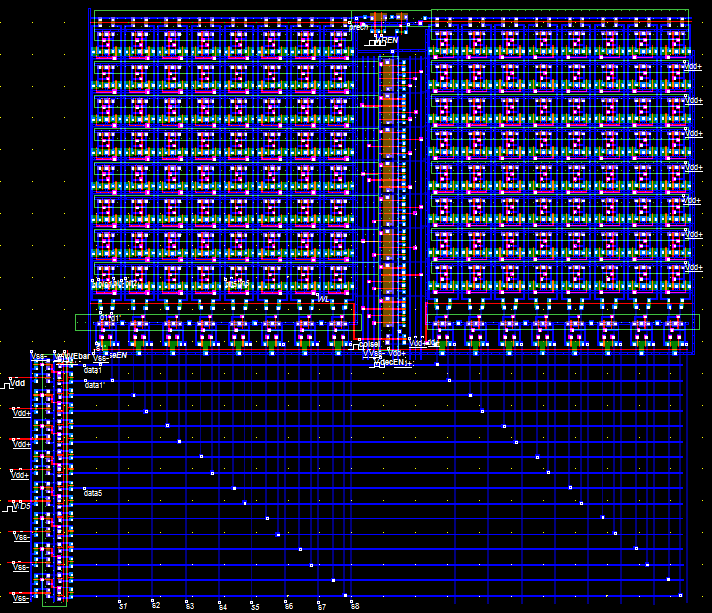
|  |  |  |
| --- | --- | --- |
| Parameter | 6T | 4T |
| Avg. Write power | 25.6µW | 14.49µW |
| Avg. Read power | 42µW | 12.25µW |
| Avg. static power | 13.743µW | 16.495µW |
| Avg. write delay | 0.093nS | 0.068nS |
| Avg. Read delay | 0.074nS | 0.096nS |

**Table [6.2] Simulation results for 6T and 4T SRAM Cache**

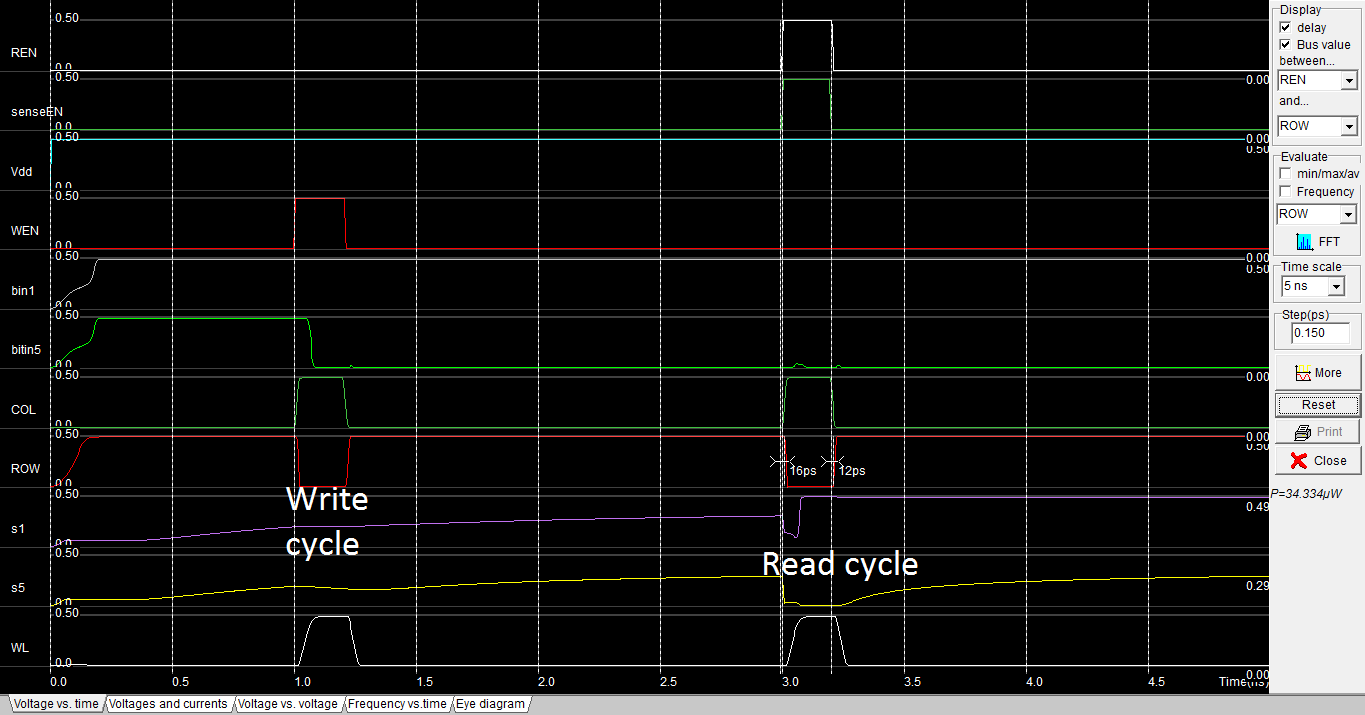
Decrease in average write and read powers are 44% and 71% respectively. Here average static power of 4T is increased by 20% due to the excess power consumed by sense amplifier used in 4T cache. This is not a major factor to be considered, as the size of the array increases the power consumed by sense amplifier becomes negligible. Whatever may be the size of array number of sense amplifiers required will be equal to the word size and the power consumed by them will become just a fraction of total power.

Average access delay of 4T cache is less compared to 6T. At this point it appears that 6T SRAM can be replaced by 4T because power delay product of 4T is less, but the problem here is maximum access delay of 4T. The maximum access delay of 4T cache is 0.2nS where as for 6T cache it is 0.106nS in case of read '1'. This reduces the maximum frequency at which 4T cache can be operated.

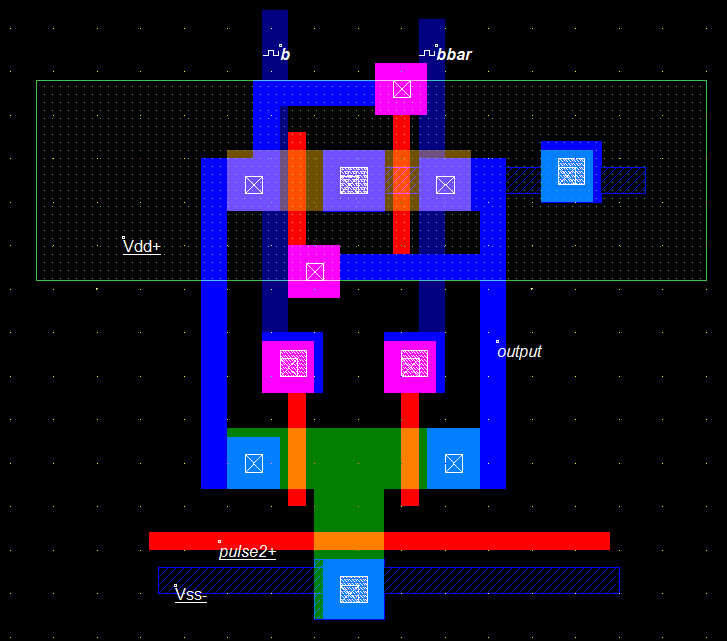
By decreasing the maximum access delay of 4T cache it can be assured that 4T can provide better power delay product than 6T. Using “Divided bit line” technique this delay can be reduced.



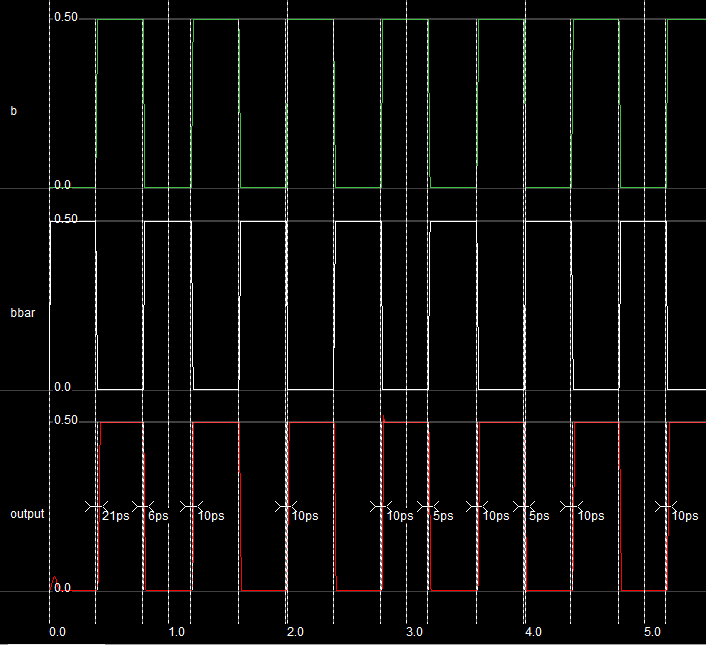
**Fig (6.5) Layout of 6T cache**

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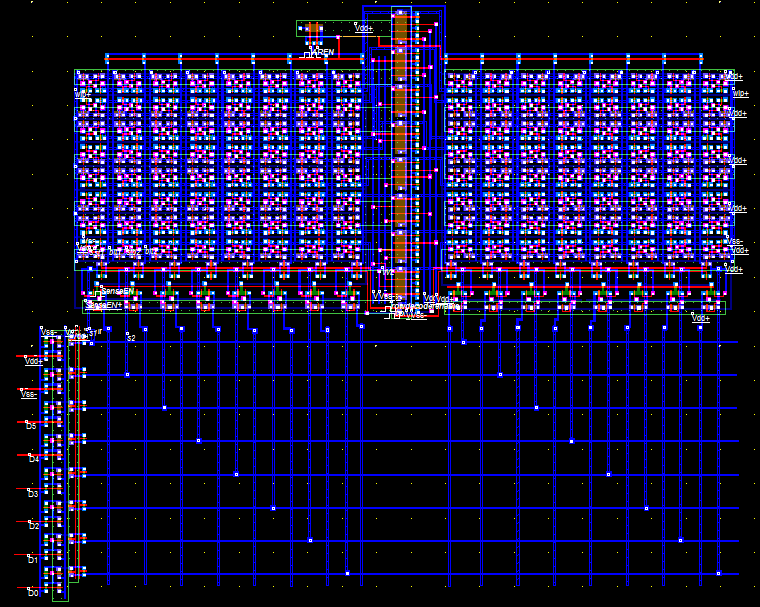
**Fig (6.6) Simulation waveforms for 6T Cache**



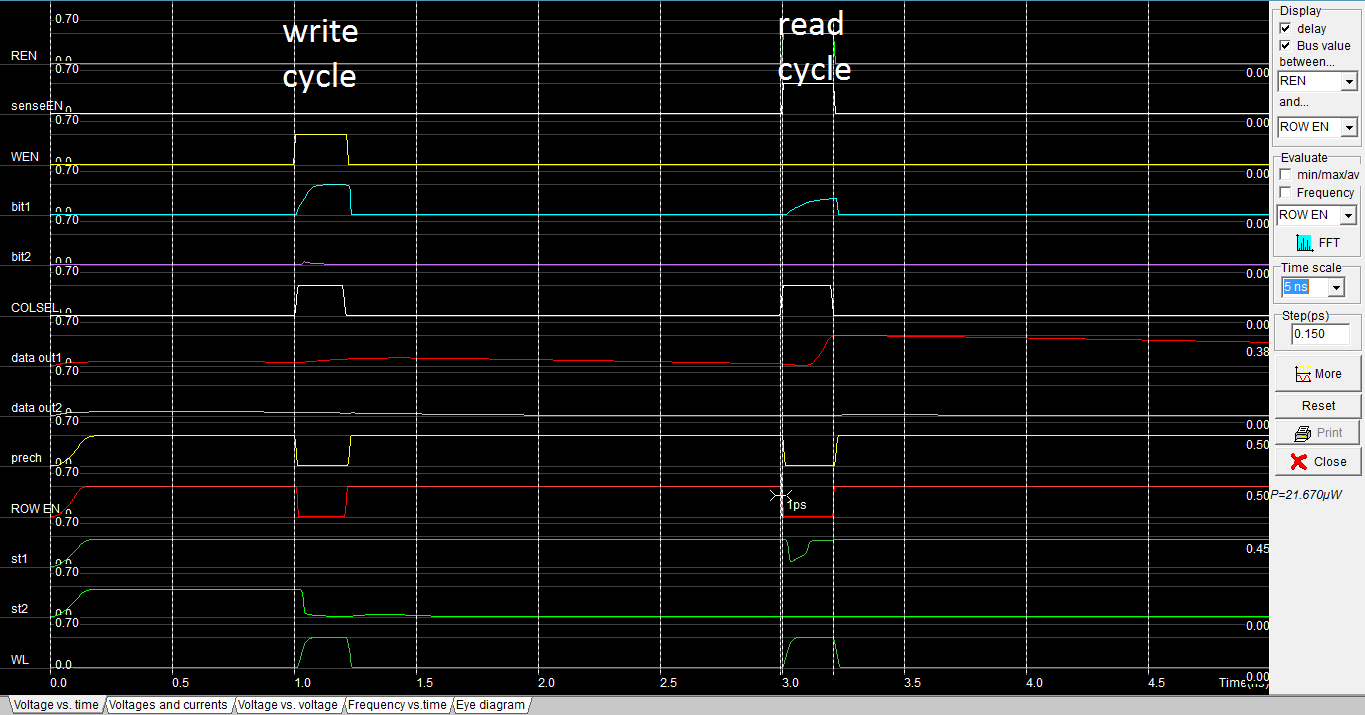
**Fig (6.7) Layout of 6T Sense Amplifier**



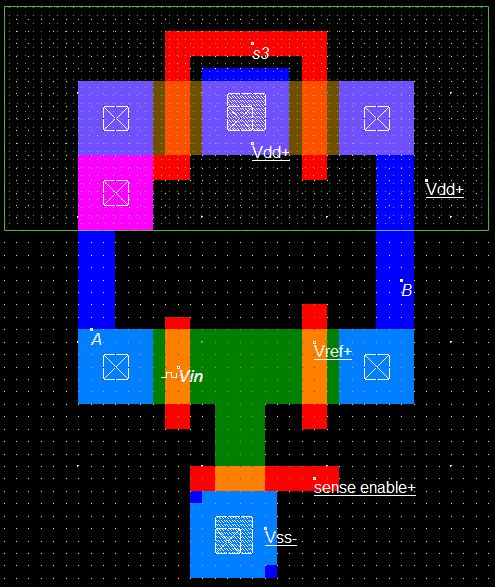
**Fig (6.8) Simulation waveforms of 6T Sense Amplifier**



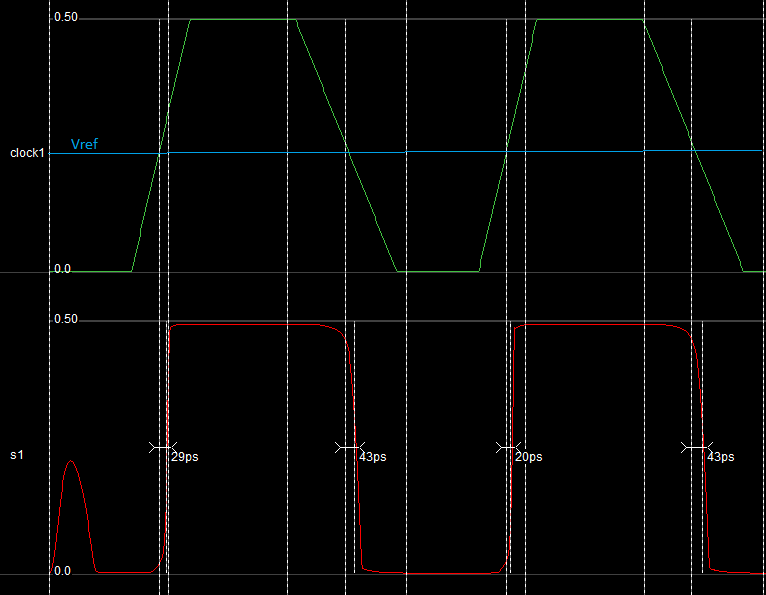
**Fig (6.9) Layout of 4T SRAM Cache**

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**Fig (6.10) Simulation waveforms for 4T SRAM Cache**

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**Fig (6.11) Layout of 4T Sense Amplifier**

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**Fig (6.12) Simulation waveforms of 4T Sense Amplifier**

**6.3 DIVIDED BIT LINE COMPARISON**

In divided bit-line technique cells are grouped to decrease the access delay. Optimal number of cells are grouped to attain maximum reduction in delay. Simulation results for modules with and without divided bit line technique are as follows.

|  |  |  |
| --- | --- | --- |
| Parameter | Single bit line | Divided bit lint |
| Avg. Write power | 17.164µW | 15.75µW |
| Avg. Read power | 16.027µW | 16.54µW |
| Avg. write delay | 0.236nS | 0.22nS |
| Avg. Read delay | 0.28nS | 0.21nS |
| Power delay product(Write) | 4.05 | 3.465 |
| Power delay product (Read) | 4.51 | 3.47 |

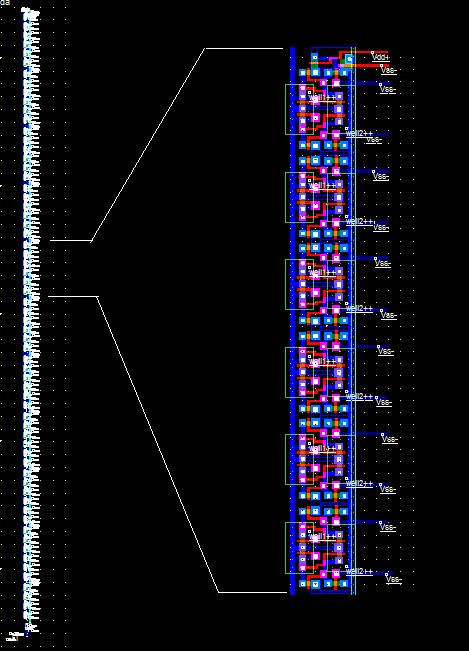
**Table [6.3] Simulation results for and 4T single bitline and divided bit line**

By implementing divided bit line technique power delay product for write cycle is improved by 14.5% and for read cycle improvement is 23%. The problem of maximum delay in the case of read '1' is reduced by 52.5%. Observations show that in case of '0' there is not much variation in delay values but for '1' write and read delays are reduced to half of the original value. Therefore by using 4T SRAM and divided bit line technique together a low power cache memory can be designed without much compromise in operation speed.

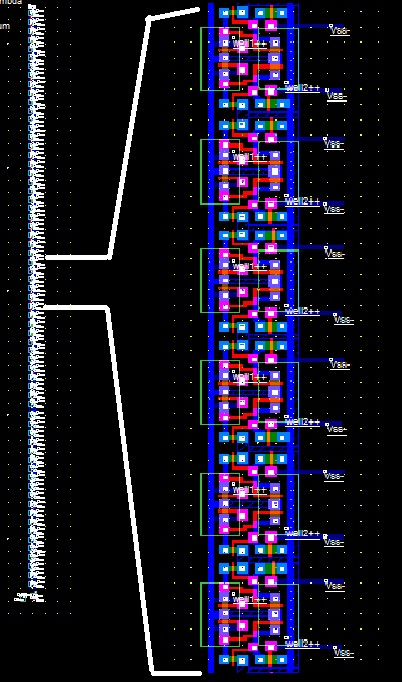
Divided bitline technique is applied for a few values of M to verify the graph obtained in Fig (5.3). These results obey the graph.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Parameter M | M=8 | M=10 | M=12 | M=14 | M=16 | M=20 |
| Avg. Write power(µW) | 15.92 | 15.79 | 15.758 | 16.225 | 16.06 | 15.769 |
| Avg. Read power(µW) | 16.51 | 16.52 | 16.54 | 16.08 | 16.14 | 16.27 |
| Avg. write delay (nS) | 0.239 | 0.2245 | 0.22 | 0.231 | 0.233 | .249 |
| Avg. Read delay(nS) | 0.213 | 0.2145 | 0.21 | 0.285 | 0.21 | 0.238 |
| Power delay product(Write) (µW-nS) | 3.804 | 3.544 | 3.466 | 3.75 | 3.74 | 3.926 |
| Power delay  product (Read) (µW-nS) | 3.516 | 3.543 | 3.47 | 4.58 | 3.389 | 3.87 |

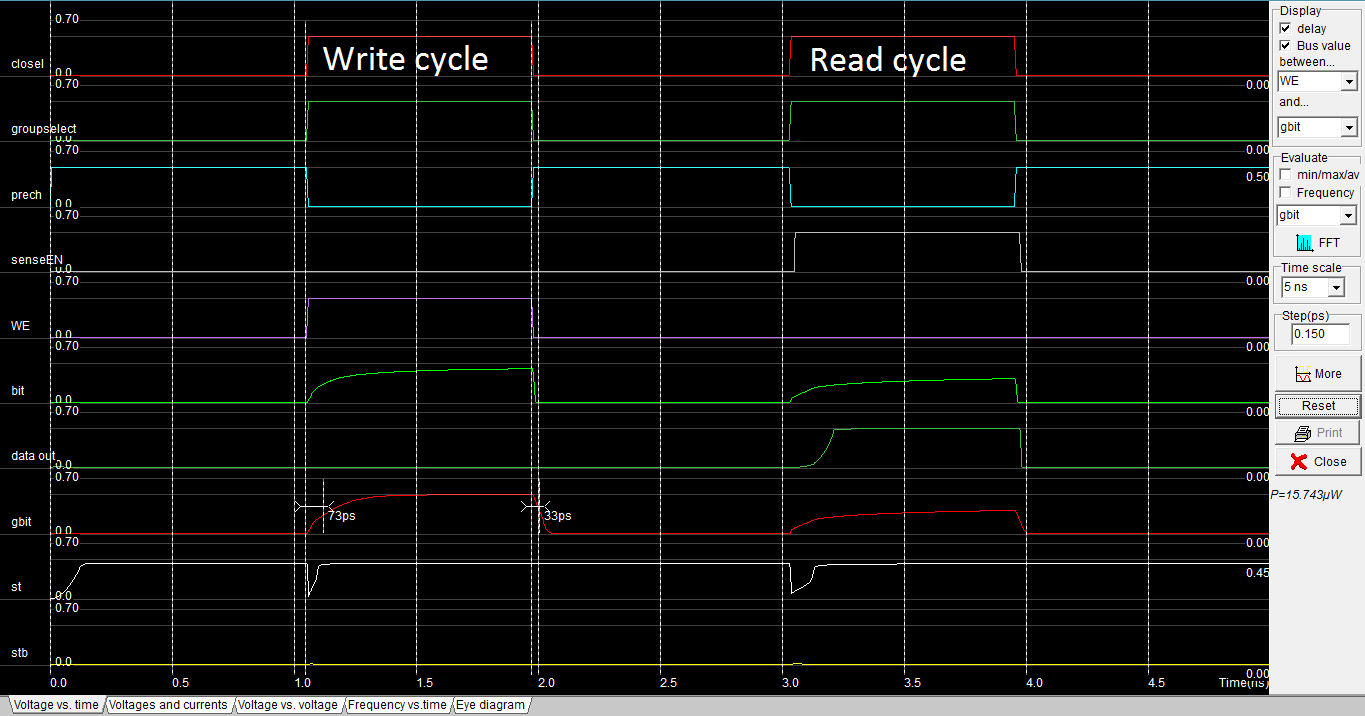
**Table [6.4] Simulation results for 4T divided bitline for different values of M**



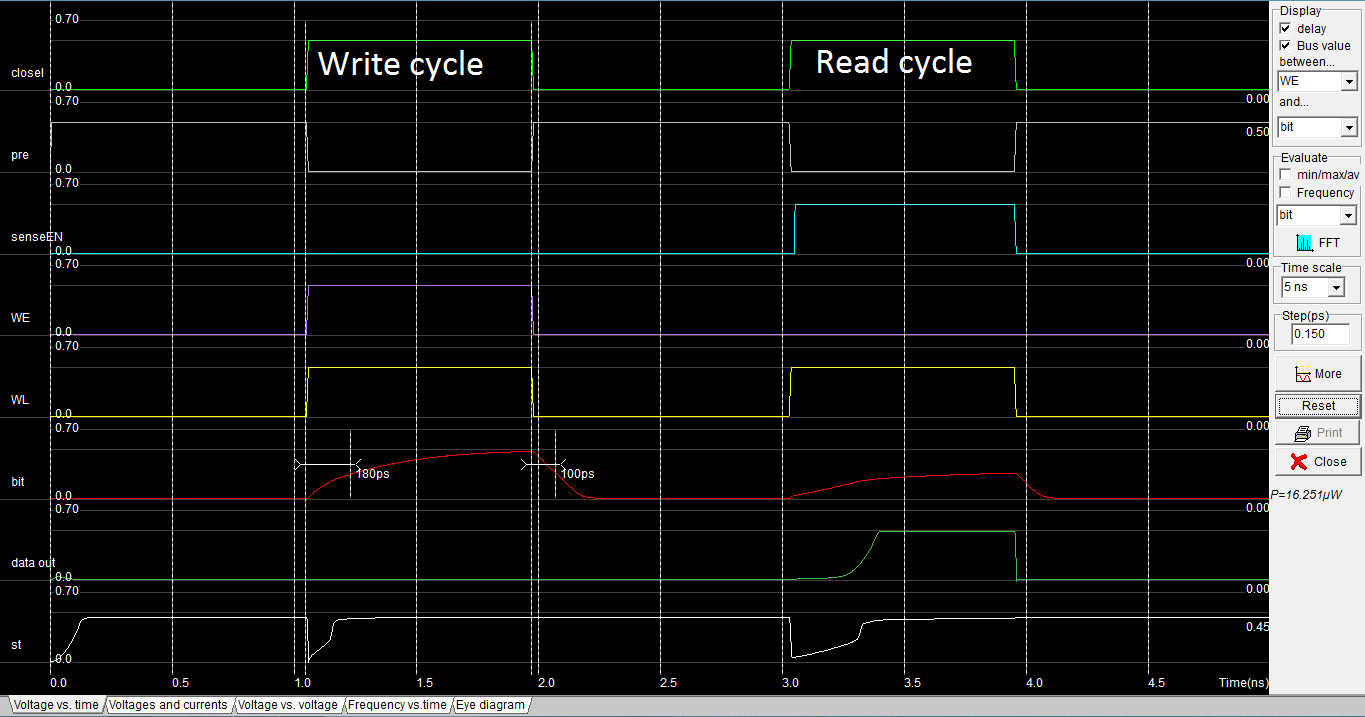
**Fig (6.13) Layout of 4T divided bitline M=12**

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**Fig (6.14) Layout of 4T single bitline**



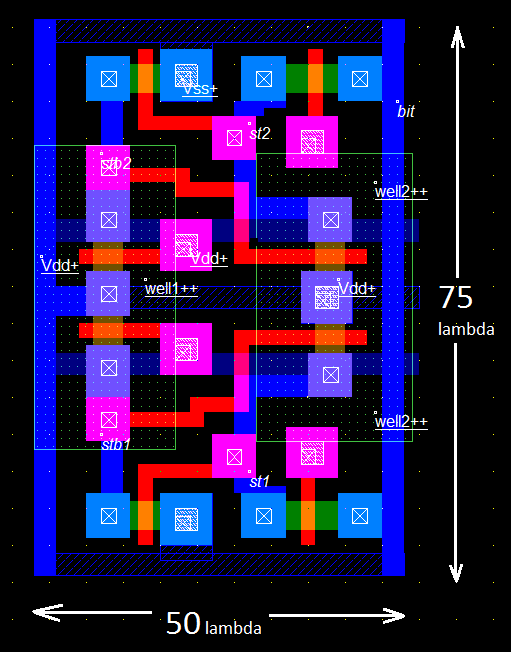
**Fig (6.15) Simulation waveforms for 4T divided bitline M=12**

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**Fig (6.16) Simulation waveforms for 4T single bitline**

**6.4 AREA COMPARISON**

In 4T SRAM Cell two N-wells are used, this will increase area the cell. The design of the 4T SRAM allows us to merge drains of load and access transistors with those of the cell above it in the array. When the drains of load and access transistors with those of the cell above it in the array are merged effective area of each less will be less than a 6T SRAM cell.

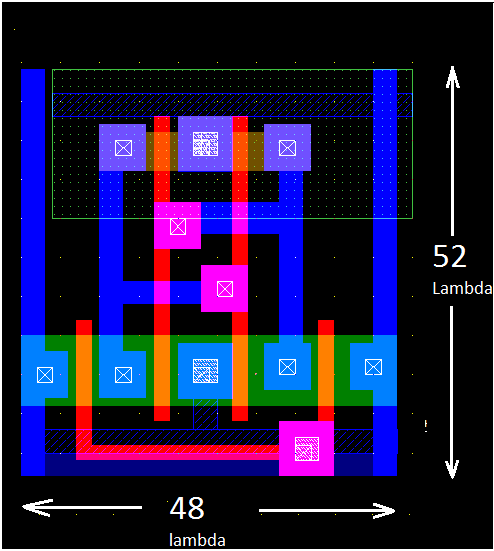


**Fig (6.17) Layout of 2 4T SRAM cells with dimensions indicated**

Area of the above 2 cells is 50 λ \*75 λ = 3750 λ2 ; where 2λ= 50nm.

Since this is the area of two cells the effective area of one cell will be

3750 λ2 /2 =1875 λ2



**Fig (6.17) Layout of a 6T SRAM cell with dimensions indicated**

The area of the 6T SRAM cell shown above is

52 λ \* 48 λ = 2496 λ2

Comparing the areas of 6T and 4T SRAM cells

=.7512 =75.12%

Therefore 4T SRAM cell is about 75% of 6T SRAM cell. There is reduction in area of about 25%.

**6.5 SUMMARY**

In this chapter 6T and 4T SRAM cells and Cache memories are simulated and compared for various parameters like power, delay and area. Results show that 4T cache consumes less power and area when compared to 6T cache but gives more delay. Delay reduction is achieved by employing divided bitline technique. Comparison results of 4T single bitline and 4T divided bitline show that access delay has reduced after the application of this technique.